

# BROADBAND PACKET SWITCH PROCESSOR

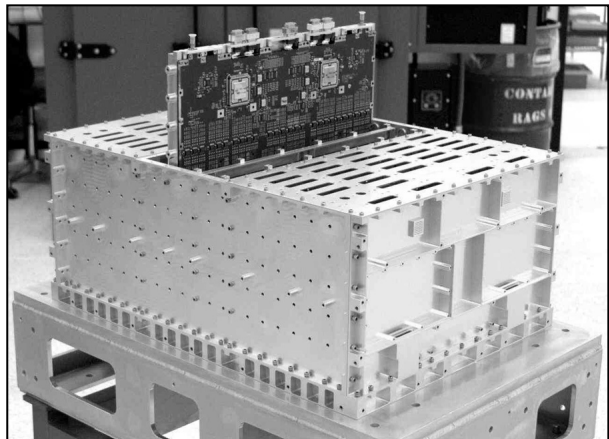
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## ABSTRACT

This paper presents an overview of the architecture for a broadband, high-speed packet switch processor used in the TRW Gen\*Star system. The first application of the Gen\*Star design is the Astrolink program. TRW is currently in production of the 4th generation of digital communications processors. Features and benefits of several key capabilities of the processor design for space applications are presented in this paper. The high-speed packet switch processor uses standard asynchronous transfer mode (ATM) cell structure, which conveys all the Quality of Service (QoS) characteristics of ATM to the Gen\*Star network. A non-blocking crossbar switch with overspeed and input arbitration optimizes switch performance and alleviates output port contention. The downlink has output priority queues with programmable downlink scheduling and adaptive coding that provides maximum flexibility for traffic control and QoS. The resource control function is a distributed architecture using a two-layer approach that maximizes performance vs. weight and power.

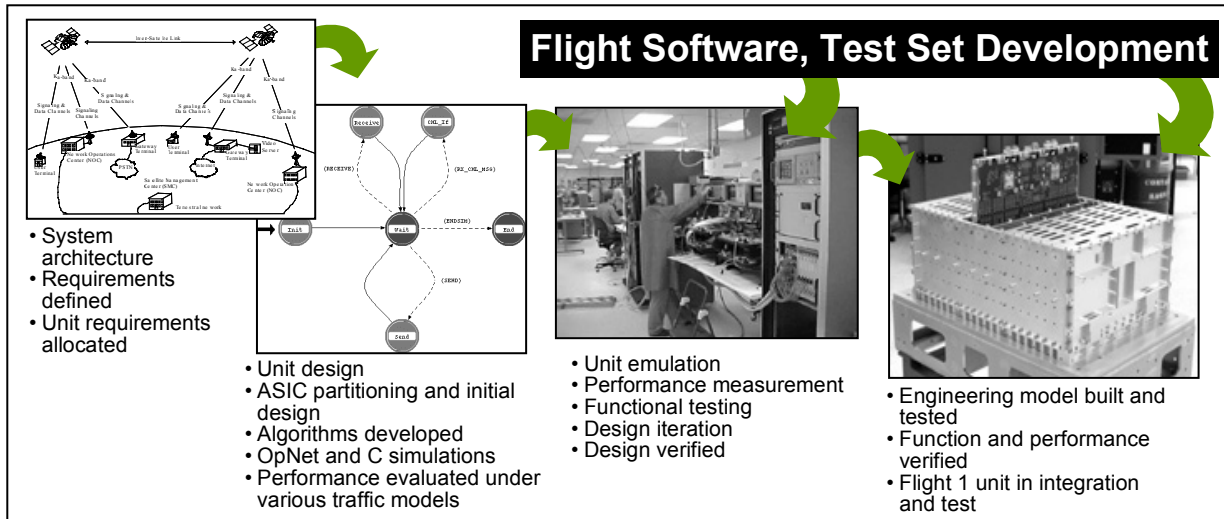
## INTRODUCTION

TRW has been a leader in processed payload for satellites—now in its 4th generation of production. The current generation of payloads is designed to address the commercial satellite broadband market and is built around a central broadband packet switch (Figure 1). In making ATM the networking backbone of the new generation of communication satellites, it will provide a true multimedia network, including services such as point to point, realtime, bi-directional voice connection, digital audio on demand with compact disc (CD)-like quality, which includes audio broadcasting. Video teleconferences, broadcast video, video on demand are all services that can be provided with this communication satellite system, as well as seamless interface to Internet and web-browsing applications.



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**Figure 1. Broadband Packet Switch Processor Design Verification Unit**

TRW has developed a broadband packet switch based on the Gen\*Star system. As shown in Figure 2, this development started with an architectural trade study to develop a system concept from which the switch requirements could be allocated. Network simulations were used to validate the design under a variety of traffic models. Detailed simulations and hardware emulations were used to ensure complete functionality, system throughput, congestion management, and predictable QoS. As of this writing, engineering model validation is complete, and the first Astrolink flight unit is in integration and test.



**Figure 2. Packet Switch Development Process**

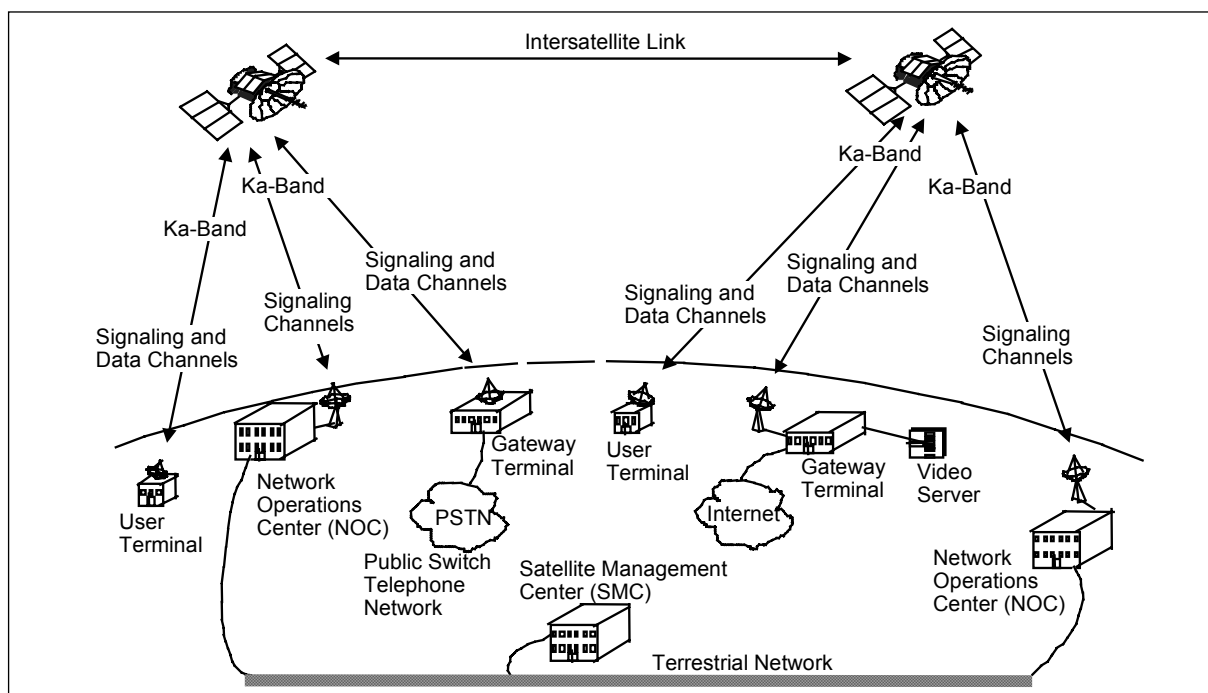
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Processed payloads are very competitive with respect to the bent-pipe transponder system in many ways. The ability to encapsulate any data over the ATM permits efficient transport of voice, data, multimedia, or specific applications yet to be defined. By incorporating built-in-self-test (BIST) into the hardware, both the unit and payload level integration is greatly simplified as compared to analog testing of an intermediate frequency (IF) switch. Using the latest design tools, digital design can be completed successfully faster than analog design and has enabled the building of a flight-like design verification model (DVM) payload in a span comparable to bent pipe payloads. The processor switch also allows multiplexing multiple signals destined for a downlink beam to be multiplexed into a single, high-rate data stream. This can be transmitted using a high efficiency saturated traveling wavetube amplifier (TWTA) at much lower power consumption than an equivalent multi-channel per carrier signal through a TWTA that is backed off.

The ATM has emerged as a leading technology for high-speed packet switching, especially in implementing broadband integrated digital service networks (BISDNs), as well as other high-speed communication networks. ATM technology allows the ease of integration for a wide variety of networking applications on a common switching and transmission infrastructure, including classical data applications, web-browsing, realtime audio and image applications, such as video on demand. TRW has furthered this technology by implementing it onto a communication satellite system. With ATM as the backbone of the data network, the entire satellite communications network can be managed and controlled with standard network control applications. Effective communication linkage is thus provided between users on the ground through user terminals, and various ground networks through gateway terminals and network operations centers (NOCs).

Figure 3 shows the concept of operations for a satellite network using the broadband packet switch processor as the onboard broadband packet switch processor. A ground user (a user terminal or gateway terminal) negotiates with the NOC to request a connection. The NOC then sends commands to the on-board router to establish the negotiated connection with the desired destination terminal. The satellite management center (SMC) communicates with various NOCs worldwide to ensure proper operation of the entire satellite system.

The ATM cell switching architecture offers flexibility and compatibility with existing protocols and interfaces. It is extremely scalable—serving the needs of individual users requiring very little bandwidth as well as those with high bandwidth demands, such as large business users over a single network infrastructure. The switch implementation conforms to ATM standards, allowing the unit testing to be performed by commercial off-the-shelf (COTS) test equipment. The ATM network also enables QoS guarantees, which provides realtime and non-realtime, and both constant bit-rate (CBR) and variable bit-rate (VBR)



**Figure 3. Satellite Network Concept of Operations**

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services. It also offers negotiated QoS guarantees for each connection for a variety of traffic data through the network.

TRW has built this broadband packet switch processor around a distributed system architecture (shown in Figure 4), to provide:

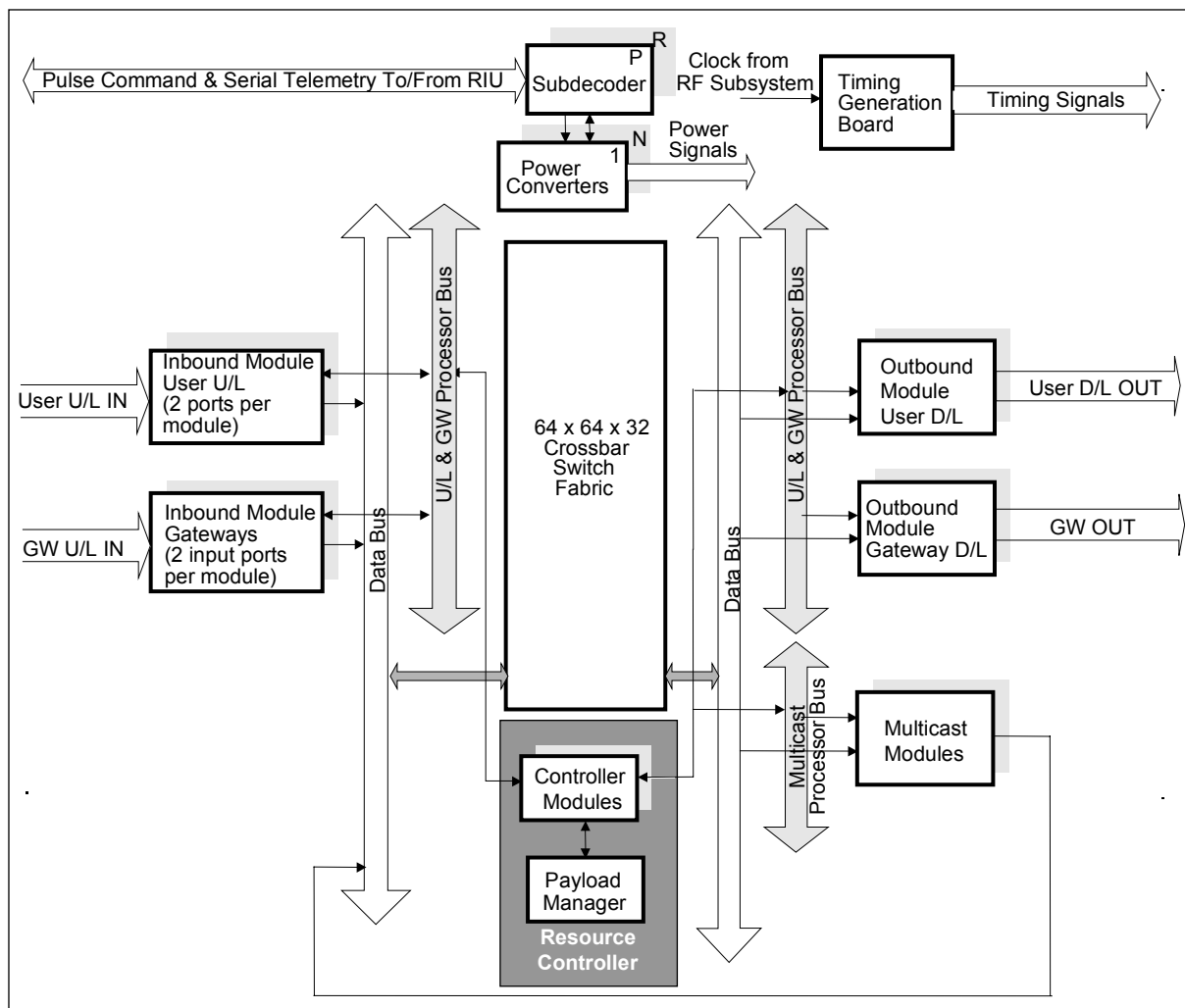
- Unicast switching—point-to-point connection
- Multicast switching—point-to-multi-point connection
- Modularity and scalability—accommodates up to 128 input ports and 128 output ports
- High performance—a fully loaded system that can sustain data rates greater than 10 gigabits/second (Gbps) net of all overhead
- Quality of service—system delivers priority-based congestion control, dedicated low latency queuing, and preservation of packet sequence

The following sections discuss in greater detail various architectural features of this broadband packet switch processor.

### INPUT ARCHITECTURE

Input processing architecture of the broadband packet switch processor focuses on preprocessing the incoming ATM cell traffic of various connection types for switching to their desired output port. Features of the input architecture include:

- Processes three types of connections (virtual channel (VC), virtual path (VP), and connectionless) using table lookup—offers flexibility
- Remapping of received ATM header virtual channel identifier (VCI) to an output VCI—enables full address reuse per port pair and simplifies network control
- Header error control (HEC), error check, and generation—ensures data integrity
- Receives traffic from two demodulator inputs per module—enables more processing capability with less hardware; thus provides a savings in power and weight



**Figure 4. Satellite Network Concept of Operations**

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- Idle cell discard—allows more efficient data traffic processing and preserves downlink bandwidth for useful data
- Interface to onboard processor—processes ground commands, e.g., call setup and/or tear-down and fault management
- Collection of statistics—enables performance monitoring and fault management, e.g., number of cells received and cells dropped due to HEC error; queue occupancy and queue overflow; single- and double-bit error counts and memory locations; and activity monitors for fault management and isolation
- Arbitration of head of line (HOL) cell
- Scalable and expandable

The input architecture is easily scalable by using the same design for all types of input processing whether it is a user terminal or a gateway terminal. The architecture is easily adaptable to the needs of the network; one can increase or decrease the number of input processing modules as needed with increasing or decreasing uplink beams without affecting other parts of the packet switch processor. Each module's capability to interface to and process data from two demodulators simultaneously leads to power and weight savings onboard the satellite.

## ARBITRATION AND SWITCH FABRIC ARCHITECTURE

Data is routed across a  $64 \times 64$  self-routing, non-blocking crossbar switch fabric, sitting at the heart of the packet switch processor where any input port can route to any output port. The switch has a speedup factor to minimize contention. Each input processing module has the capability to process two data inputs from two uplink beams simultaneously, and each output processing module is also capable of processing data for two downlink beams; thus, the architecture can have up to 128 input ports as well as 128 output ports.

A central arbitration scheme is an integral and necessary part of this architecture to resolve any conflicts that may arise when more than one input port wants to send data to the same output port. The fair arbitration algorithm is optimized to minimize the probability of input queuing congestion while still ensuring no ports are starved for service.

## OUTBOUND ARCHITECTURE

The output processing architecture of the broadband packet switch processor focuses on the post-processing of ATM cell traffic for downlink transmission. The architecture is optimized for a space-based application, with large cell buffers to feed the downlink beams in order to minimize dropped cells due to congestion. Features of the output architecture includes:

- Queuing by downlink priority and adaptive coding
- Multi-level downlink priorities based on QoS needs—accommodates up to 512 different queues and supports the TRW-developed fair-weighted queuing algorithms optimized for space applications
- Adaptable coding modes per weather conditions—allows heavy coding for rain or storm conditions and light coding for clear weather greatly increasing the usable capacity while maintaining high link availability
- Flexible downlink frame forming—supports the fair-weighted queuing algorithms, processes data for two downlink beams simultaneously, and reconfigures the downlink scheduling table based on ground and onboard processor commands
- HEC—error check ensures data integrity
- Network congestion control—prevents loss of high priority data during traffic congestion, uses cell loss priority (CLP) bit for cell discard, and supports early packet discard (EPD)
- Multiple modes of queue structure—dynamic link list structure maximizes flexibility of queue space and priority data processing and fixed partitioning structure guarantees queue space for all priorities
- Statistics collection—enables performance monitoring and fault management, e.g., queue occupancy, queue thresholds, and peak cell count; CLP and EPD cell discard counts; amount of free cell space in queue; number of cells transmitted; and activity monitors for fault management and isolation
- Scalable and expandable

The output architecture is easily scalable by using the same design for all types of output processing, whether it is downlink to a user terminal or a gateway terminal. The architecture is also easily adaptable to the needs of the network, one can increase or decrease the number of output processing modules as needed with increasing or decreasing downlink beams without affecting other parts of the packet switch processor. With each module's capability to process data for, and interface to, two downlink beams simultaneously, it leads to power and weight savings on board the satellite.

## MULTICAST ARCHITECTURE

Maximum efficiency is achieved using uplink bandwidth by having the multicast capability onboard the satellite. The terminals need only to send the data once to the satellite, then let the onboard packet switch processor perform the duplication; thereby, allowing the uplink bandwidth to be used efficiently for non-duplicated data. The multicast architecture is a cross between input and output architectures. Its input is from the switch fabric output port and its output is to the switch fabric input port. The multicast architecture features include:

- ATM cell replication for transmission to multiple destinations—allows maximum and most efficient usage of uplink bandwidth
- HEC error check and generation—ensures data integrity
- Processing of three types of connections (VC, VP, and connectionless) using table lookup—offers flexibility
- Interface to onboard processor—processes ground commands, e.g., multicast traffic call setup and/or tear-down, addition or deletion of multicast destinations, and fault management
- Collection of statistics—enables performance monitoring and fault management, e.g., number of cells received and/or cells dropped due to HEC error; number of cells duplicated; queue occupancy and queue overflow; single bit error and double bit error counts and memory locations; and activity monitors for fault management and isolation
- Arbitration of HOL cell
- Scalable and expandable

The multicast architecture, like the input and output architectures, is easily scalable and expandable, and its implementation will not affect changes to other parts of the overall switch architecture.

## DESIGN APPROACH

Supporting 70+ beams and >10 GBPS throughput requires extremely dense packaging including the use of advanced microelectronics. Complex, multi-million gate, sub-micron complementary metal oxide semiconductor (CMOS) application-specific integrated circuits (ASICs) make onboard processing realizable within the satellite's weight and power allocation. TRW has implemented a design methodology during its four generations of digital processors that ensures "first pass success" of the designs. This includes extremely thorough and rigorous design verification prior to design hand-off to the foundry, early functional prototyping of multi-ASIC functions, and use of advanced tools to ensure all the intricacies of sub-micron CMOS design are accounted for. Traditional functional testing will not ensure adequate fault coverage, so BIST is incorporated into the designs allowing thorough and rapid test at both piece-part and unit level. The complexities of ASIC designs are mitigated by the measures taken during design flow. The unit architecture supports line replaceable modules (LRMs). Each individual module is replaceable at the payload level without impacting other modules.

## SUMMARY

TRW's Gen\*Star broadband high-speed packet switch processor addresses the future needs of the broadband processed payload market. The architecture allows maximum flexibility as well as maximum scalability. A variety of applications and services can be accommodated by this architecture. Design verification is completed and production is underway.