BROADBAND MULTIBEAM FDMA/TDMA DIGITAL CHANNELIZER/DEMODULATOR

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ABSTRACT

This paper presents an overview of the architecture for a broadband multibeam, multichannel frequency division multiple access/time division multiple access (FDMA/TDMA) digital demodulator that is a key component of the TRW Gen*Star system. The uplink traffic in a 125 MHz sub-band is processed by identical—and independent—demodulation module processors. These demod modules are responsible for the channelization, demodulation, decoding, time synchronization and power control of uplink signals.

This paper will present features and benefits of several key components of the demodulator design. Leveraging a TRW-configurable, digital channelization architecture (patent pending), a range of terminal sizes—from inexpensive fractional T1 terminals to high bandwidth 150 Mbps terminals—is supported within the system. Exploiting an additional benefit of the nature of the digital algorithm, guard bands between the frequency channels are not required allowing more efficient use of the uplink bandwidth.

The onboard demodulator is responsible for carrier phase ambiguity resolution and tracking in the presence of frequency errors and performs coherent quadrature phase shift keying (QPSK) demodulation of each TDMA burst in each frequency channel. Furthermore, synchronization, power control, and demodulation algorithms are described that are critical to minimizing cell loss rate (CLR) in a burst uplink environment. Finally, the paper concludes with a summary of predicted and measured performance data for the engineering model demodulator.

BACKGROUND

The Gen*Star system developed by TRW Inc. provides digital communication between terminals located worldwide using satellite payload and asynchronous transfer mode (ATM) switch technology. This system is comprised of a constellation of satellites, each containing an advanced communications payload forming the space segment, a ground segment consisting of various Earth terminals with satellite dish antennas, and an operations center that controls the system operation. The use of advanced digital processing onboard the satellite provides system subscribers with services and performance unsurpassed by any satellite system fielded to-date. By incorporating the ATM switching functions in the satellite, system users may communicate directly without the need of a ground-based hub. The first application of the Gen*Star payload is in the Astrolink system.

TRW has developed a broadband multibeam FDMA/TDMA digital channelizer/demodulator based on the Gen*Star system. As shown in Figure 1, this development started with an architectural trade study to develop a system concept from which the channelizer/demodulator requirements could be allocated. Analyses, simulations, and hardware emulation were used to ensure complete functionality and near theoretical performance. As of this writing, engineering model validation is complete and the first Astrolink flight unit is in integration and test.

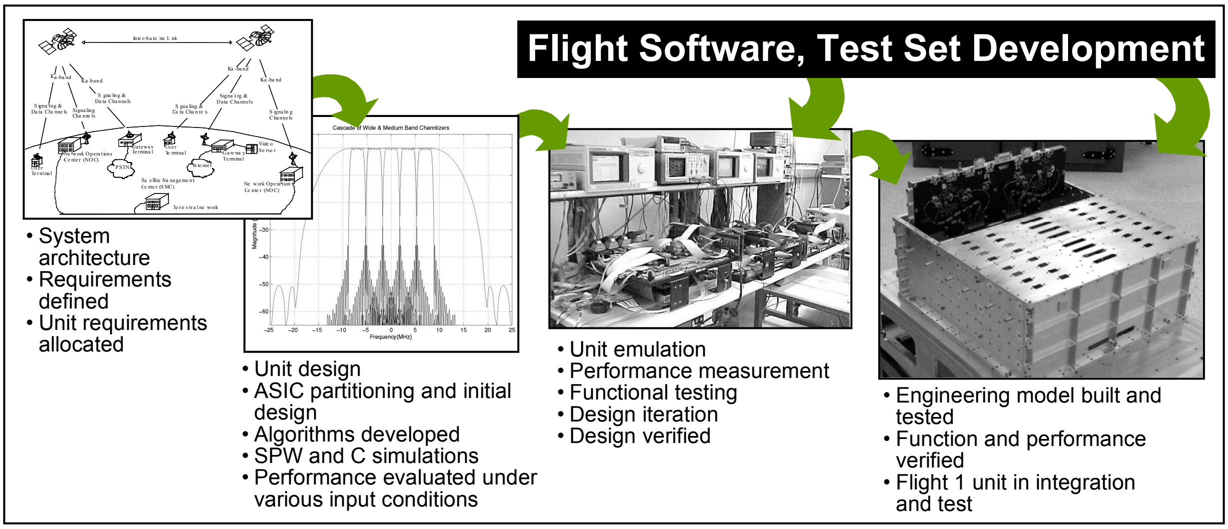

Figure 1. Demodulator Development Process

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The user terminal (UT)-to-payload (PL) uplink operates in the Ka-Band (28.35–30.0 GHz) that is divided into contiguous frequency sub-bands, each 125 MHz in bandwidth. The UT-PL uplink access scheme is FDMA/TDMA, wherein each frequency sub-band is divided into multiple frequency channels. The temporal axis of each frequency channel is divided into frames and further partitioned into multi-user access time slots. Each UT transmits to the PL on one or more time slots within each frame on possible multiple frequency channels.

The UTs group four ATM cells together and encodes the block code using a Reed-Solomon block code. An optional Reed-Muller code may also be applied to provide additional coding gain when link margins are reduced by atmospheric absorption or interference. The encoded block is then scrambled using a programmable code to 'whiten' the transmitted waveform. Finally, the data is demultiplexed and QPSK-modulated with square root raised cosine (SRRC) filtering in the desired frequency channel.

The timeframe is portioned into slots for traffic data blocks and time probes, both of which are assigned by the operations center to the terminals. Time probes are pseudo noise (PN) sequences that are transmitted by the UTs to acquire and maintain timing synchronization. The system uses long-loop timing control in which the terminals adjust the transmit clocks so signals arrive at the satellite symbol synchronous to the spacecraft reference. The time probes are measured by the satellite and a timing report is sent back to the UTs to maintain synchronization. This scheme minimizes the amount of guard time between TDMA time slots and reduces burst overhead in the uplink waveform.

A special channel is provided for entry probes used by the UTs to gain initial access to the system. This is a special slotted ALOHA channel in which the UTs transmit a short request message. The system responds with a coarse timing adjustment as well as an initial time probe slot and traffic TDMA slot assignments.

UPLINK DIGITAL CHANNELIZER DEMODULATOR OVERVIEW

The 125 MHz sub-bands are downconverted from Ka-Band to an intermediate frequency using MMIC amplifiers and downconverters. Each of these downconverted sub-bands are serviced by independent but identical demodulation processing modules. Except for an analog bandpass filter and some interface gain elements, all demodulation functions are performed digitally using low cost CMOS technology. Employing a single wideband analog-to-digital converter (ADC), the entire 125 MHz sub-band is digitized and then processed in a single CMOS application specific integrated circuit (ASIC).

The demodulation ASIC is partitioned into two main functional sections as shown in Figure 2. The channelizer functional section separates the FDMA channels from the single wideband

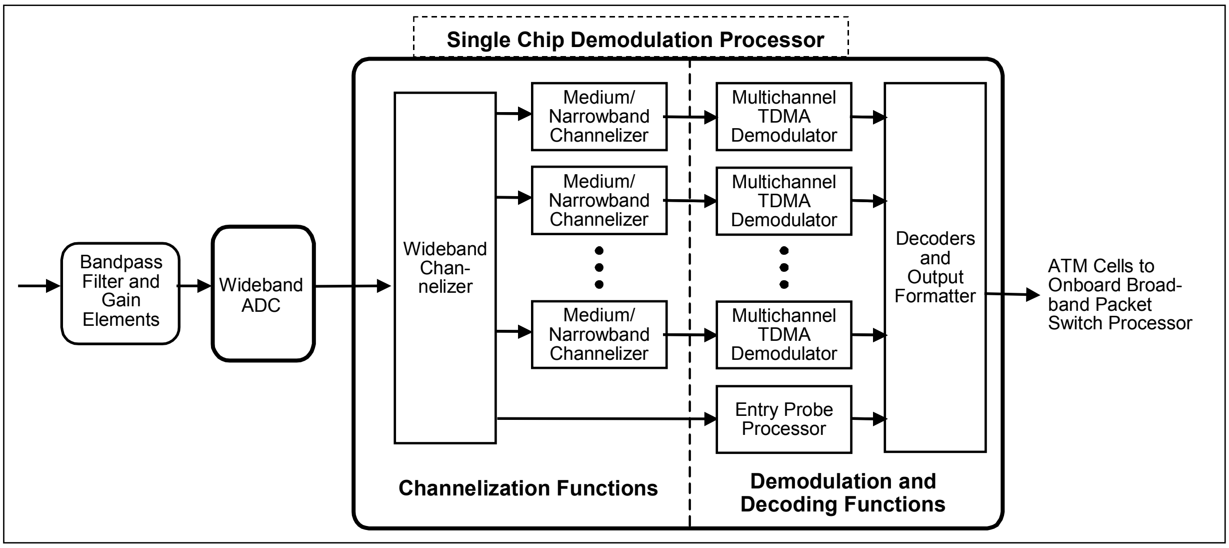

Figure 2. Demodulation Processing Module Architecture

digitized sub-band. Following the channelizers is a bank of multi-channel TDMA demodulators and decoders that can be programmed to process the wide, medium, and narrow band channels of the input. Additionally, the channelizer section also feeds an entry probe block to process the initial requests from the terminals for access to the system. The decoder and output formatter block then decodes the traffic blocks, formats the time probe and entry probe reports, and multiplexes all ATM cells into a single output datastream to the onboard broadband packet switch processor.

Each demodulator ASIC contains the processing required to flexibly channelize, demodulate, decode and synchronize all 175 broadband channels within a beam, the system equivalent of a cable modem or DSL hub. To accomplish this, the channelizer/demodulator ASIC is composed of 5.5 million gates and performs 34 giga-operations per second.

DIGITAL CHANNELIZATION

Separation of the input frequency channels is performed in a computationally efficient multi-stage digital channelizer. Computational efficiency is much more important in a space-borne processor than in a ground-based processor due to the severe power constraints on a satellite. This channelizer employs novel algorithms (patents pending) that dramatically reduce ASIC gate count, power consumption and power dissipation, while providing uncompromised performance and flexibility. Several TRW-developed concepts are employed to provide flexibility in decoupling the channel frequency spacing and filter decimation factor that are usually linked in traditional channelizer design. This offers the ability to optimize the frequency band for efficient spectral management.

The architecture provides flexibility in routing the user signal to any of the medium/ narrowband channelizers or directly to the demodulators. Additionally, any channel can be directed to the entry probe processor for simultaneous processing. The entry probe channel is typically placed in a wideband channel along with active traffic data.

The channelizers implement the channel select filters using digital finite impulse response (FIR) structures. These filters exhibit the most desired effect of linear phase processing, which eliminates implementation loss due to signal dispersion. With the digital implementation, we have excellent control of the inband ripple and stopband attenuation. Coupled with the precise control of the filter band channel spacing of the channelizer algorithm, guard bands between the frequency channels are not required allowing for a more efficient utilization of the uplink bandwidth. Figure 3 shows the cascade response of the channelizer architecture for the case of medium band channels. The outer line represents the response of one of the wideband

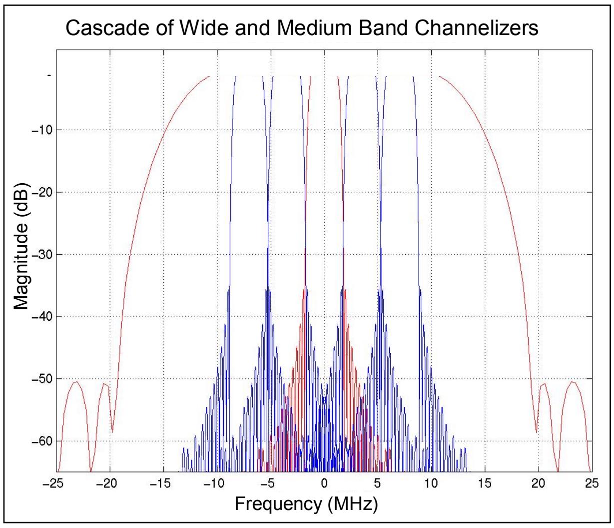

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Figure 3. Multi-Stage Channelizer Filter Response Example

channelizer outputs. The filter exhibits a flat response over the passband of interest and has >50 dB of stopband rejection for adjacent channels. Response of the five channels of the second-stage, medium-band channelizer is also shown. This filter response has very steep transition regions to enable close stacking of the communication channels, which maximizes efficiency of the available spectrum.

The channelizer architecture offers system providers the flexibility to portion the 125 MHz sub-band to the particular needs of their customers in that beam. Since each beam is handled by an independent processor, each beam that services a different geographic region can be dynamically optimized for that region. A subset of any 125 MHz band can be reconfigured without affecting the service in the remaining portion of the band allowing providers to adapt to the needs of a dynamic traffic model. Additionally, channels within a 125 MHz sub-band can be turned off and allocated to another beam providing substantial throughput flexibility in response to temporal demand fluctuations.

Following the channelization functions, each of the separated FDMA channels are processed by a bank of multi-channel demodulators. An all-digital enhanced second order loop is incorporated to perform coherent QPSK demodulation of each TDMA burst in each frequency channel. Additionally, the design includes features to allow the loop to be time shared across several channels when medium and narrowband channelization is employed reducing the required hardware implementation cost.

A functional diagram of the demodulation function is shown in Figure 4. The time probe processor is activated during the small portion of the frame dedicated to time probes. Using an algorithm developed by TRW and optimized for satellite links, the processor measures arrival time of each probe compared to the system reference, which is maintained by the spacecraft. The results are packed into ATM cells for routing back to the ground terminals. The terminals

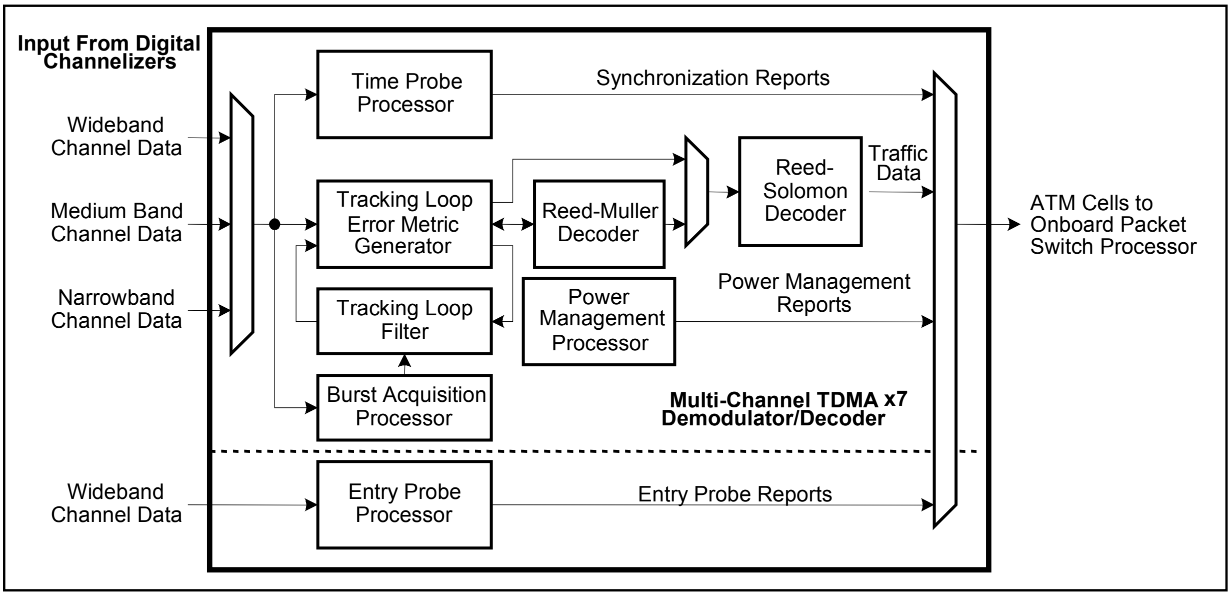

Figure 4. Functional Diagram of the Demodulation Function

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use these measurements to adaptively control their transmit symbol timing to maintain synchronization with the satellite.

Each traffic burst is first examined by the burst acquisition processor, which extracts several parameters needed for rapid acquisition and demodulation. The tracking loop error metric generator and loop filter uses a TRW enhanced architecture (patent pending) that improves performance for a satellite uplink channel. The architecture incorporates proprietary algorithms developed by TRW (patent pending) to enable reliable burst acquisition and tracking at very low SNR. Furthermore, processing is included to adaptively track frequency errors common to all traffic in a beam (Doppler) in addition to frequency errors unique to each uplink terminal thus improving system CLR.

For channels that have been assigned to terminals needing extra coding gain due to atmospheric losses, a Reed-Muller soft decision decoder is used to reduce the bit error rate. The Reed-Muller code provides enough coding gain that the demodulator cell loss ratio will satisfy the most stringent QoS levels at minimum SNR. All channels are processed by a Reed-Solomon decoder, which can correct multiple symbol errors in the received block. A power management processor operates in the background and monitors the transmitted power of all terminals both active and standby. The processor generates ATM cell reports that are used by the terminals to adaptively adjust their transmitted power for optimal communication link performance and to minimize interference to their adjacent channel neighbors. Simultaneously, the entry probe processor monitors the assigned entry probe channel and generates an ATM cell message only when requests are received thus minimizing the amount of downlink bandwidth consumed by this overhead function. Finally, the demodulation processor module multiplexes the received traffic ATM cells from all of the multi-channel demodulations along with the various reports into a single datastream of ATM cells that is sent to the broadband packet switch processor for switching and transmission.

Figure 5 shows the measured BER performance of the multi-channel TDMA demodulator shown for both heavy coded (Reed-Muller and Reed-Solomon cascaded coding) and light coded (Reed-Solomon coding only) channels. This data is taken prior to the Reed-Solomon decoder so that the performance of the demodulator can be more sensitively perceived. Note that both the heavy and light coded channels are well behaved even with timing and frequency offsets present.

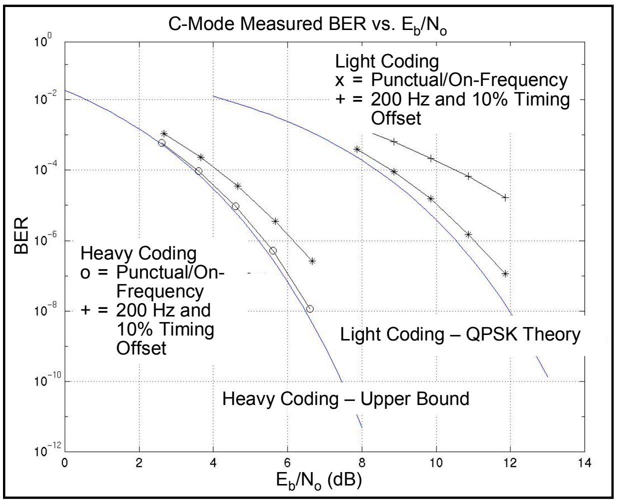

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Figure 5. TDMA Demodulator Performance

The demodulation processing modules are coupled with an onboard computer for command and control to form the demodulation unit. The subsystem is designed with a back-plane architecture and plug-in cards resulting in a modular and scalable design as shown in Figure 6. Additionally, the backplane architecture allows for easy replacement of modules that fail during test. The unit shown in the figure supports 36 125-MHz sub-band channels, however the design is easily scalable.

All of the ASICs in the demodulation unit incorporate built-in-self-test (BIST) circuitry in the designs. Due to the large size and complexity of the demodulation ASIC, traditional ASIC test methodologies would fall short of acceptable fault coverage requirements. The BIST allows thorough (>98 percent fault coverage) and rapid test at all levels of integration from wafer probe through unit test. A special test bus and interface in the unit enables the BIST circuitry to be executed once the ASICs and boards have been installed in the unit to reverify system

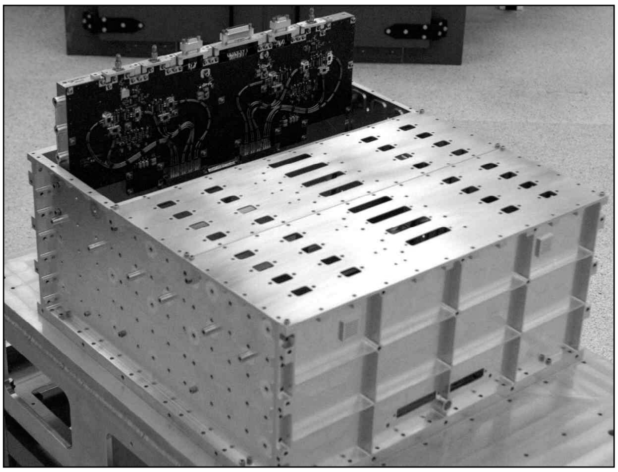

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Figure 6. Uplink Demodulation Unit Plug-in Style Cardcage

health. Interconnect between ASICs and boards can be verified using the boundary scans of the ASICs via the test bus. This is used extensively during unit integration and test to quickly identify manufacturing defects and to reduce system test time.

Supporting many 125 MHz sub-bands—and up to 175 frequency channels per sub-band—requires extremely dense packaging including the use of advanced microelectronics. Complex, multi-million gate, submicron CMOS ASICs make onboard processing realizable within the satellite's weight and power allocation. TRW has implemented a design methodology during its four generations of digital processors that ensures "first pass success" of the designs. This includes extremely thorough and rigorous design verification prior to design hand-off to the foundry, early functional prototyping of multi-ASIC functions, and use of advanced tools to ensure all intricacies of the submicron CMOS design are accounted for.

Various simulation tools and detailed analysis are used to predict performance and validate the VHDL code. Even with the largest code accelerators, it is impossible to simulate enough time to thoroughly verify functionality of the uplink timeframe and characterize the performance. The rapid prototyping methodology developed and employed at TRW allows for real analog signals generated by a terminal emulator to be processed in realtime. This complements the simulation and analysis activities and enables full performance characterization prior to committing the design to an ASIC. Since the rapid prototyping tools operate in realtime, speed increases of 1,000,000 times that obtainable through simulation are routinely obtained.

SUMMARY

The Gen*Star broadband multi-beam FDMA/TDMA digital channelizer/demodulator built by TRW includes the features and performance required to deploy a global communication system. Using advanced processing algorithms, the design supports a range of terminals from inexpensive fractional T1 terminals to high bandwidth terminals. Leveraging extensive use of digital processing and incorporating BIST architectures, the design represents a cost-effective solution for emerging broadband communication system.