Gen*Star
Results Applicable to Ka-Band

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Gen*Star Program
Results Applicable to Ka-Band Service Suppliers and End Users

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1. INTRODUCTION

The Gen*Star Satellite Network program was conceived at TRW to achieve two principle goals: (1) to provide a generic Ka-band system design and technology base; and (2) to pursue payload and system opportunities. Achieving these goals allows TRW to approach the broadband business with a network solution, leveraging our payload technology to produce a technical design that achieves the customer's business case.

Over the past several years, the Gen*Star program has included systems engineering, network simulation and analysis, payload technologies, network operations, and terminal concepts. TRW has continued to implement the Gen*Star program and has successfully built a hardware functional prototype of the payload. This paper is an update to the TRW paper, "Processing Payload Considerations for Broadband Satellite Systems," presented at the 3rd Ka-Band Utilization Conference.

This paper describes the status of TRW's Gen*Star program and the capabilities that have been developed that are directly applicable to future programs. Significant progress has already occurred in network architecture and communications design. Emulation and simulation of the payload and network are part of the Gen*Star program. A roadmap of technology developments is in place to continuously evaluate new technologies that will enhance overall network performance while minimizing risk, schedule, and cost impacts. We pay particular attention to the progress in devices that will enhance antenna design and devices that will enable intersatellite links.

After a short review of the Gen*Star payload and program, this paper describes development progress including a status of key technology areas.

2. CURRENT GEN*STAR PAYLOAD DESIGN

The Gen*Star payload was designed to provide competitive, satellite-based, on-demand broadband service. The payload consists of antennas, an RF subsystem, and a processor subsystem. To meet the requirements of a specific system, the Gen*Star payload can be scaled in processor capacity and in the number of beams a constituent satellite uses, to conform to a specific coverage pattern.

The uplink multibeam antennas receive the signals at the payload. Very low sidelobes allow four-way frequency reuse within the full-earth field of view. The low noise amplifiers and down converters (LNA/DC) are in an extremely small MMIC package mounted directly to the feeds. This package optimizes payload sensitivity and allows a low frequency IF cable interface to the payload module, simplifying integration complexity and reducing weight. The IF signals are input to the demodulators.

The demodulators immediately convert the signal to digital form. The digital samples are processed via proprietary channelization algorithms to select the three different channel types. These very efficient algorithms operate at less than half the power of typical FFT algorithms. Each channel is demodulated and decoded. Functionally they are the equivalent of well over 10,000 demodulator/decoders on board. The demodulator outputs the data formatted into ATM cells for presentation to the router.

The router is composed of an ATM switch and an on-board computer for control. Proprietary switch-scheduling algorithms maximize use of the downlink channels with minimal weight and power. Switch outputs are formatted and encoded for transmission, then modulated with offset QPSK square-root-raised cosine pulses.

Upconversion with a single carrier per TWTA allows highly efficient transmission. The carriers are input to the antenna for transmission. The antenna's high gain and low sidelobe design enables small terminals to close the link. The payload components have a legacy of successful flight use.

Antenna and RF Subsystem

The antenna subsystem is composed of four uplink and four downlink antennas of identical design. These antennas are designed to provide high gain across the coverage area with very low side lobes to minimize interference. Each antenna must scan the entire earth. The design produces very small degradation in beam shape at high scan angles. It also enables the system to provide capacity focusing into dense areas, with almost twice the capability of a standard Cassegrain or Gregorian design. Maximum use of MMIC technology allows minimum weight.

Processor Subsystem

The processor subsystem demodulates and decodes the uplink signals, and it ATM switches the data. The subsystem has been productized into a backplane architecture with plug-in cards making the design inherently modular and scaleable. As an example, multicast capability is increased by simply installing more multicast plug-ins. Likewise, the payload processor can be configured to process additional beams by simply adding additional demodulator and router plug-ins.

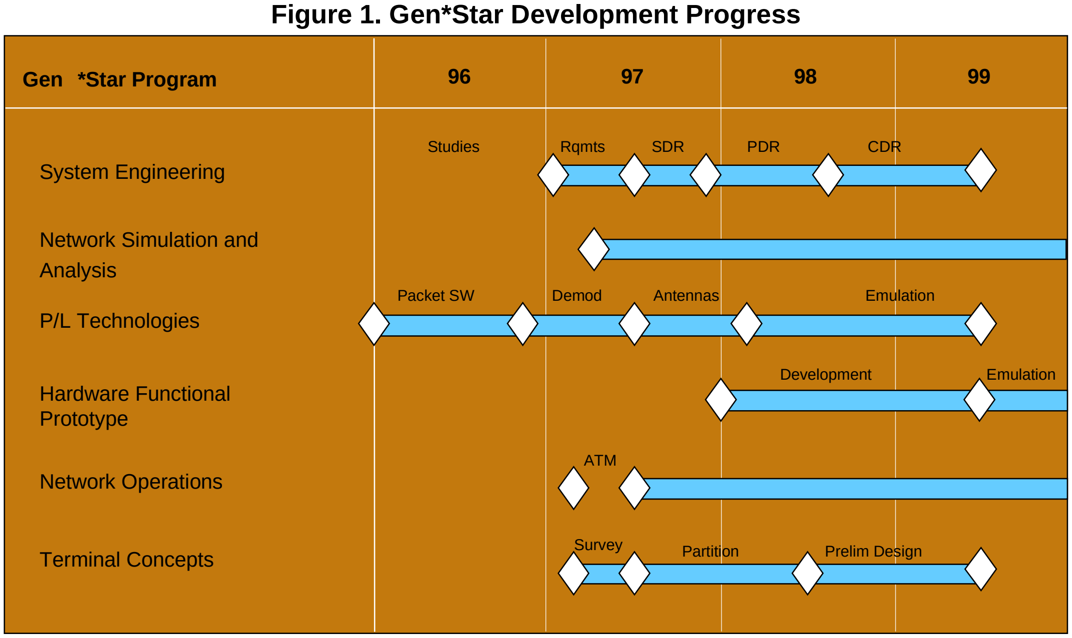
On-orbit system flexibility is achieved via programmable flight controllers and configurable processor functions. Some payload functions will benefit from being adaptable over time. Software-based functions and configurable hardware allow the payload to be optimized for changes in traffic patterns over the life of the satellite. Other software-based functions allow for continuous improvements in satellite management. Examples include security algorithms, fault management processing, and congestion control processing. For rapid fault detection and isolation, the software checks critical payload functions continuously.

A key aspect of any digital processor in space is robustness with respect to the radiation environment. In addition to well-understood total-dose lifetime degradation, the subsystem must be resistant to Single Event Upset (SEU) and catastrophic latch-up. In a system like Gen*Star, service interruption due to SEU would adversely affect customer satisfaction and public image. TRW's pioneering SEU-tolerant design work on Milstar discovered many subtle complexities and developed design processes and techniques to prevent and mitigate the impact of SEU. To avert these problems on Gen*Star, Milstar experience and lessons learned were applied. The design was analyzed, all SEU sites with potential to disrupt service were identified, and proprietary design mitigation techniques were employed. In addition, TRW has developed a fault-tolerant, radiation-hardened computer. It is SEU immune and provides for software uploads and non-intrusive trace capabilities without interruption of service.

3. GEN*STAR DEVELOPMENT PROGRESS

The Gen*Star development program was conceived to create a payload design along with its companion network and terminal design infrastructures. The Gen*Star program at TRW began in 1996 with system engineering studies of payload technology (P/L) development based on TRW and government heritage programs. The program consists of development work in systems engineering, network simulation and analysis, payload technologies, network operations, and terminal concepts. Figure 1 describes the salient elements of the Gen*Star development schedule. The Gen*Star network architecture was refined and OPNET-simulated to firm up its technical foundation and close the business case. System description, CONOPS, and system specification documents were created to facilitate transition of the Gen*Star design to development programs.

Figure 1. Gen*Star Development Progress



4. CURRENT GEN*STAR DEVELOPMENTS AND STATUS

With respect to the Development Program, the most relevant areas of technology development are occurring in payload-related areas. This paper will discuss the payload emulator, network emulation, payload technologies, antenna development, and optical intersatellite link terminals.

Payload Emulation

TRW has developed a Gen*Star payload hardware functional prototype (HFP) to verify and emulate the design and operation of the payload. This HFP can be adapted to prototyping any broadband multimedia satellite network and can be used to measure performance of the payload in the network. The HFP is driven by stimulus and response equipment (SRE), which simulates the external interfaces to the Ka-band payload.

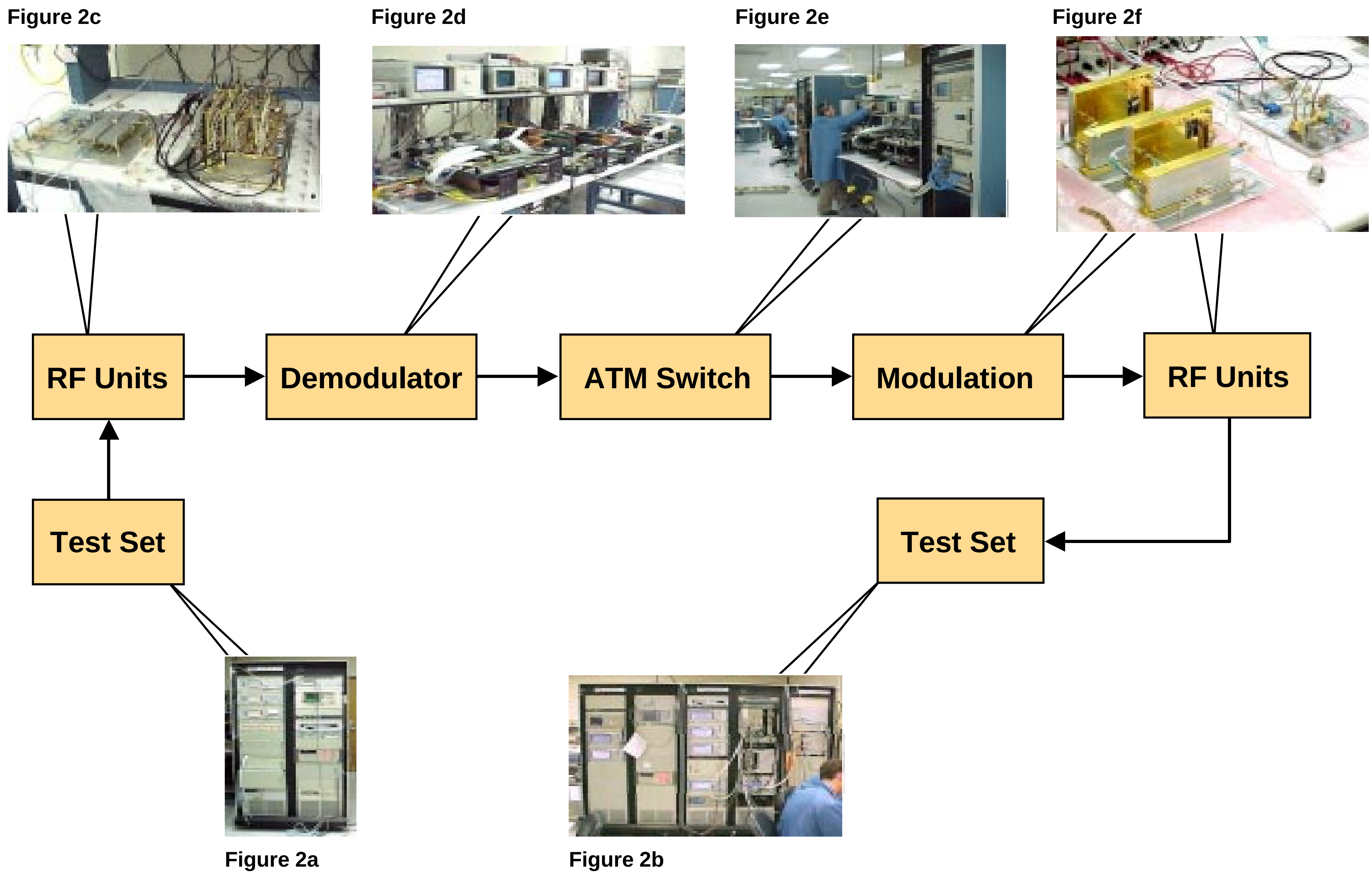
The HFP was an internal TRW development. The same top-down engineering approach used on our many space systems programs was applied. Our System Engineering group analyzed payload requirements, performed detailed partitioning trades, and flowed requirements and interface definitions to all components. Additionally, a configuration control board was established to manage changes. The block diagram for the HFP is shown in Figure 2. While the flight payloads will have more beams, we needed to build only enough processing chains to demonstrate interference effects, flow and congestion control, etc. To those ends we developed two end-to-end processing chains. The central ATM switch has four channels, two of which can be directly loaded from the test-set. The HFP test-set was architected from the individual unit test-sets, allowing us to “break in” at any point to isolate functionality and performance (Figure 2a and 2b).

The HFP input is at 30 GHz and starts with a brassboard integrated millimeterwave assembly (IMA) containing the 30 GHz LNA and downconverter (Figure 2c). This component contains four MMIC designs, the most critical of which is the 0.1µ HEMT LNA. The component was fabricated, tested, and integrated into the HFP. It meets all gain and noise figure requirements. After some filtering, the next key component is the C-band downconverter (Figure 2c). This unit tunes each LNA/downconverter output to the appropriate sub-band and downconverts it to the A/D I/F frequency.

The signal is then input to the processor subsystem. This subsystem was developed in a “sea of gates” with numerous large field programmable gate arrays (FPGAs). All the digital design was done in VHDL. By the use of VHDL and by partitioning the overall functionality into generic macros, we made the design completely portable to the most capable space-qualified digital technology available at the time.

The first component of the processor subsystem is the demodulator (Figure 2d). The signal is A/D converted and channelized by highly efficient FFT algorithms. Then each of up to 175 channels is demodulated, in each of the two demodulators. The demodulated symbols are then decoded and packaged for delivery to the ATM switch. In addition, all the algorithms required for system entry and acquisition have been implemented and tested.

Figure 2. Fully Operational HFP



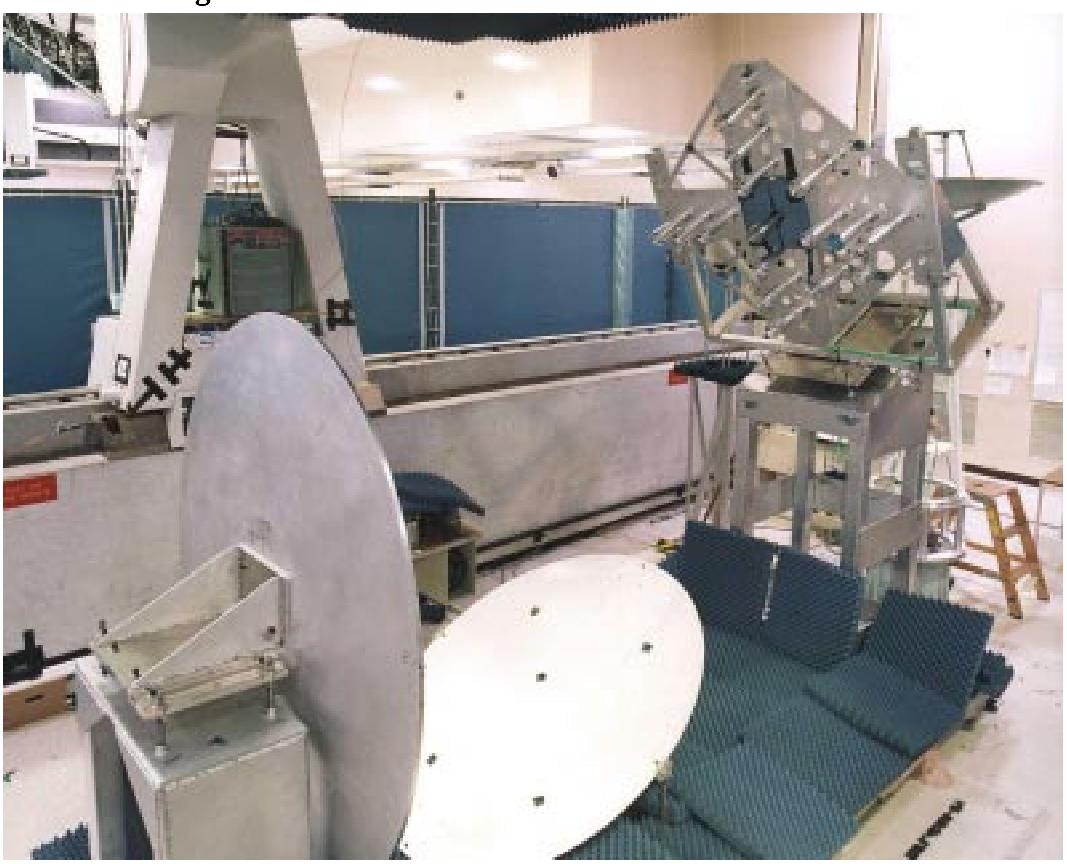
The next component in the processor subsystem is the ATM switch (Figure 2e); it accepts ATM streams from four sources (two actual demodulators and two test-set inputs). ATM headers are read, contention resolution is performed, and the cells are routed to output modules. Here the cells are queued by QoS, scheduled for the output, framed, and formatted.

The demodulators and ATM switch are controlled by an architecture of space-qualified RH32 computers. Software was developed in C++ to demonstrate the controllability of the hardware. The processor subsystem was the a critical part of the HFP, and a lot of attention was given to design reviews and test results. In all, over 3 million new design gates were developed, tested, debugged, and are functioning as expected.

The output of the ATM switch goes to the modulators (Figure 2f). The modulator accepts I and Q data, along with the synchronizing clock from the ATM switch. It then QPSK modulates the data and filters with a square-root-raised cosine (SRRC) shape. This signal is then sent to the brassboard 20-GHz upconverter (Figure 2f). The IMA contains three MMIC designs. This 20-GHz signal then can go directly to the test set or go through a 20-GHz TWTA. Local oscillator signals and clocks for all components are generated and distributed by the frequencies generator. Based on a stable 5-MHz reference, all frequency chains were designed, fabricated, and meet purity and spurious requirements (Figure 2b).

In addition to this end-to-end electronics prototype, we developed a brassboard antenna (Figure 3). Antenna performance is most crucial to payload performance so detailed analysis models

Figure 3 Gen*Star Brassboard Antenna



were developed to perform design trades and predict performance. After the design was fabricated and tested, initially the performance did not agree with the analytical predictions and there was concern that we didn't have a model with adequate fidelity. Detailed videogrammetry measurements found an error in the surface shape of the main reflector. When that surface shape was input to the analytical model the results matched the test data. The brassboard reflector surface shape was then corrected and the antenna was retested. The results then matched the originally predicted performance values.

Finally, all objectives of the HFP were met or exceeded. The end-to-end payload design has been validated. This design now provides a platform for network emulation and new technology evaluation.

Network Emulation

TRW's network emulation approach uses the payload HFP to simulate the major Gen*Star ATM switch requirements. The Gen*Star simulation test bed ties together the functions of the Network Operations Center prototype (NOC), the satellite with payload, the ground terminal prototype, the gateway terminal prototypes, and the Satellite Operations Center prototype. Simulations including Call Admission Control (CAC) and Demand Assigned Multiple Access (DAMA) requirements have been completed. The purpose of these simulations is to determine the quality of service (QoS) and throughput performance, as well as network operational performance.

Payload Technologies

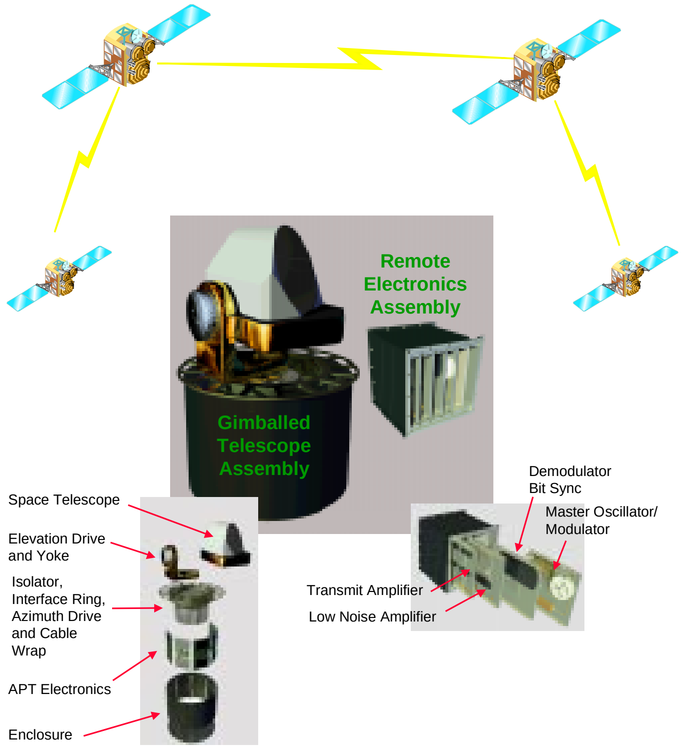
TRW maintains a technology roadmap of the key technologies that are involved in the Gen*Star Program. These technologies expand the capabilities of all segments of the program – payload, network, and terminals – and include MMIC, power amplifiers, A/D converters, ASICs, and intersatellite links.

Optical Intersatellite Link Terminals

Optical intersatellite link (OISL) terminals connect satellites in a constellation to provide regional or global networks. For the military, they can minimize dependence on vulnerable ground stations. For commercial systems, they can free users from dependence on permanent leased lines or satellite circuits, thus lowering costs. For all systems they can reduce the ground infrastructure needed to control the satellites while offering dramatic increases in flexibility to route services to users and to manage system capacity.

During the past few years, TRW has made substantial progress retiring all significant risks for optical intersatellite links (OISLs). The size, weight, and power advantages of OISL links over RF links make OISLs the preferred system choice for interconnect rates above approximately 50 Mbps. TRW has been making substantial investments in optical product development since 1996. These investments reflect TRW's commitment to laser links. We have product options with rates to 12.8 Gbps and ranges to provide a GEO-to-GEO interconnect. Figure 4 illustrates TRW's OISL product. It consists of the telescope and the related mechanical and electrical assemblies.

Figure 4. Optical Intersatellite Link Terminal



SUMMARY

TRW has invested in the development of a Gen*Star Program to enable internal developments of payload and network technology and to assist customers who are evaluating the readiness of the present technology as well as assessing the impact of future technology on current designs.

The Gen*Star development program began in 1996 and covers the payload and the design of the network and user terminals. Design effort is complemented with a payload hardware functional prototype and the development of a testbed with simulation capability.

The Gen*Star program has continuing initiatives with the development of key technologies, including digital processors, array antennas, and optical intersatellite links, that affect the space segment, the ground segment, and terminal developments of the future. Dramatic performance improvements in key technology devices are expected in the next several years.