

# FLEXIBLE AND SCALABLE PACKET SWITCH PROCESSOR ENABLES SATELLITE NETWORK ARCHITECTURES

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## ABSTRACT

This paper presents an overview of the architecture for a broadband, high-speed packet switch processor used in the TRW Gen\*Star broadband system concept. The first application of the Gen\*Star design is the Astrolink program. TRW is currently producing its 4th generation of digital communications processors. Features and benefits of several key capabilities of the processor design for space applications are presented in this paper. The high-speed packet switch processor uses standard asynchronous transfer mode (ATM) cell structure, which ensures compatibility with terrestrial ATM networks. A non-blocking crossbar switch with overspeed and input arbitration optimizes switch performance and alleviates output port contention. The downlink has output priority queues with programmable downlink scheduling and adaptive coding that provides maximum flexibility for traffic control and Quality of Service (QoS). The resource control function is a distributed architecture using a two-layer approach that maximizes performance within available weight and power.

## INTRODUCTION

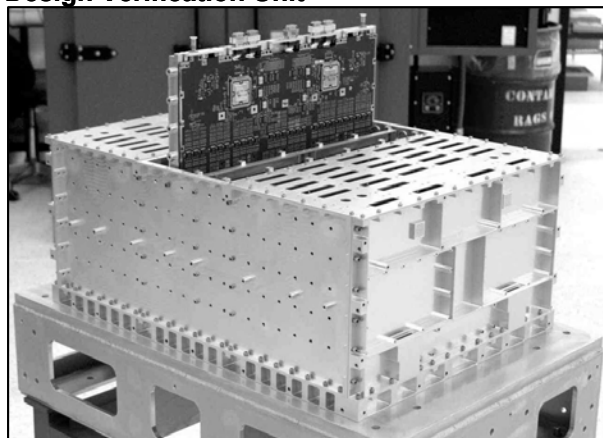
TRW has been a leader in processed payloads for satellites—now producing its 4th generation of processors. The current generation of payloads is designed to address the commercial satellite broadband market and features a central broadband packet switch. The design verification of a broadband packet switch processor has been completed (Figure 1) and the first flight production unit for Astrolink has been completed. By making ATM the networking backbone of the new generation of communication satellites, it will enable a true multimedia network supporting services such as point-to-point, real-time bi-directional voice connection, digital audio on demand with compact disc (CD)-like quality and audio broadcasting. Web browsing applications, video teleconferencing, broadcast video, video-on-demand are all services that can be provided with this communication satellite system.

Regenerative (digital processed) payloads are very competitive with transparent (bent-pipe analog transponder) systems in many respects. The ability to encapsulate any data into ATM cells permits efficient transport of voice, data, multimedia, and applications yet to be defined. While it is true that the digital

processed payload sacrifices some of the waveform transparency of the traditional analog transponder architecture, onboard switching offers a tremendous advantage in network flexibility, a more valuable asset to service providers in a changing marketplace. Unlike the traditional transponder architecture, service providers are not locked-in to a fixed network topology – full mesh, hub-spoke, multi-cast and point-point networks can be simultaneously operated and continuously re-configured in response to changing market demand.

By incorporating built-in-self-test (BIST) into the hardware, unit and payload level integration is greatly simplified compared to analog testing of an intermediate frequency based analog (IF) switch. Using the latest design tools, digital design can be completed successfully faster than analog design and a flight-like design verification model (DVM) payload can be built in a span comparable to transponder payloads. The processor switch allows multiple signals destined for a common downlink beam to be multiplexed into a single, high-rate data stream, taking advantage of statistical multiplexing gains with bursty user traffic to maximize downlink throughput efficiency and, therefore, system capacity. In-addition, this stream can be amplified using a saturated traveling wavetube amplifier (TWTA) at a much higher power conversion efficiency than an equivalent multi-carrier signal through a TWTA that is backed off for linearity. Improved power efficiency translates to higher capacity for a given spacecraft/launch vehicle, or alternately, reduced launch costs for a given capacity.

**Figure 1. Broadband Packet Switch Processor Design Verification Unit**



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The ATM standard has emerged as a leading technology for high-speed packet switching, especially in implementing broadband integrated digital service networks (BISDNs), as well as other high-speed communication networks. ATM technology facilitates integration of a wide variety of networking applications on a common switching and transmission infrastructure. TRW has furthered this technology by implementing it within a regenerative communication satellite system. With ATM as the backbone of the data network, the entire satellite communications network can be managed and controlled using conventional tools. Effective communication linkage is provided between users on the ground through user terminals, and various ground networks through gateway terminals under the control of network operations centers (NOCs).

**Figure 2** shows the concept of operations for a satellite network using the onboard broadband packet switch processor. A ground user (a user terminal or gateway terminal) negotiates with the NOC, through the satellite, to request a connection. The NOC then sends commands to the on-board router to establish the negotiated connection with the desired destination terminal. The satellite management center (SMC) communicates with various NOCs worldwide to ensure proper operation of the entire satellite system.

The ATM cell based switching architecture offers flexibility and compatibility with existing protocols and

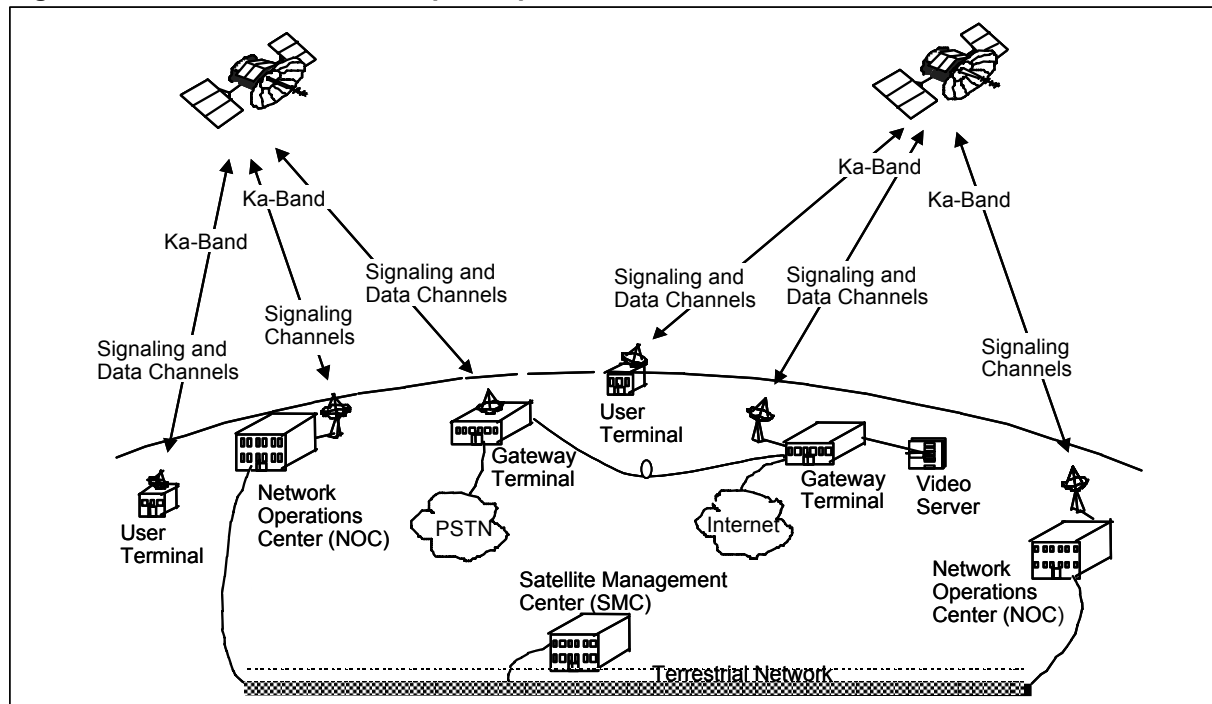
interfaces. It is extremely scalable—capable of serving the needs of individual users requiring very little bandwidth at the same time as those with high bandwidth demands, such as large business users, over a single network infrastructure. The switch implementation conforms to ATM standards, thus allowing the unit and payload testing to be performed using commercial off-the-shelf (COTS) test equipment. The ATM network also supports QoS guarantees, offering real time and non-realtime, constant bit-rate (CBR) and variable bit-rate (VBR) services, with negotiated QoS guarantees for each connection for a variety of traffic data through the network.

TRW has constructed this broadband packet switch processor using the distributed system architecture shown in **Figure 3** to provide:

- Unicast switching—point-to-point connection
- Multicast switching—point-to-multi-point connection
- Modularity and scalability—accommodates up to 128 input ports and 128 output ports
- High performance—a fully loaded system can sustain data rates greater than 10 gigabits/second (Gbps)
- Quality of service—system delivers priority-based congestion control, dedicated low-latency queuing, and preservation of packet sequence

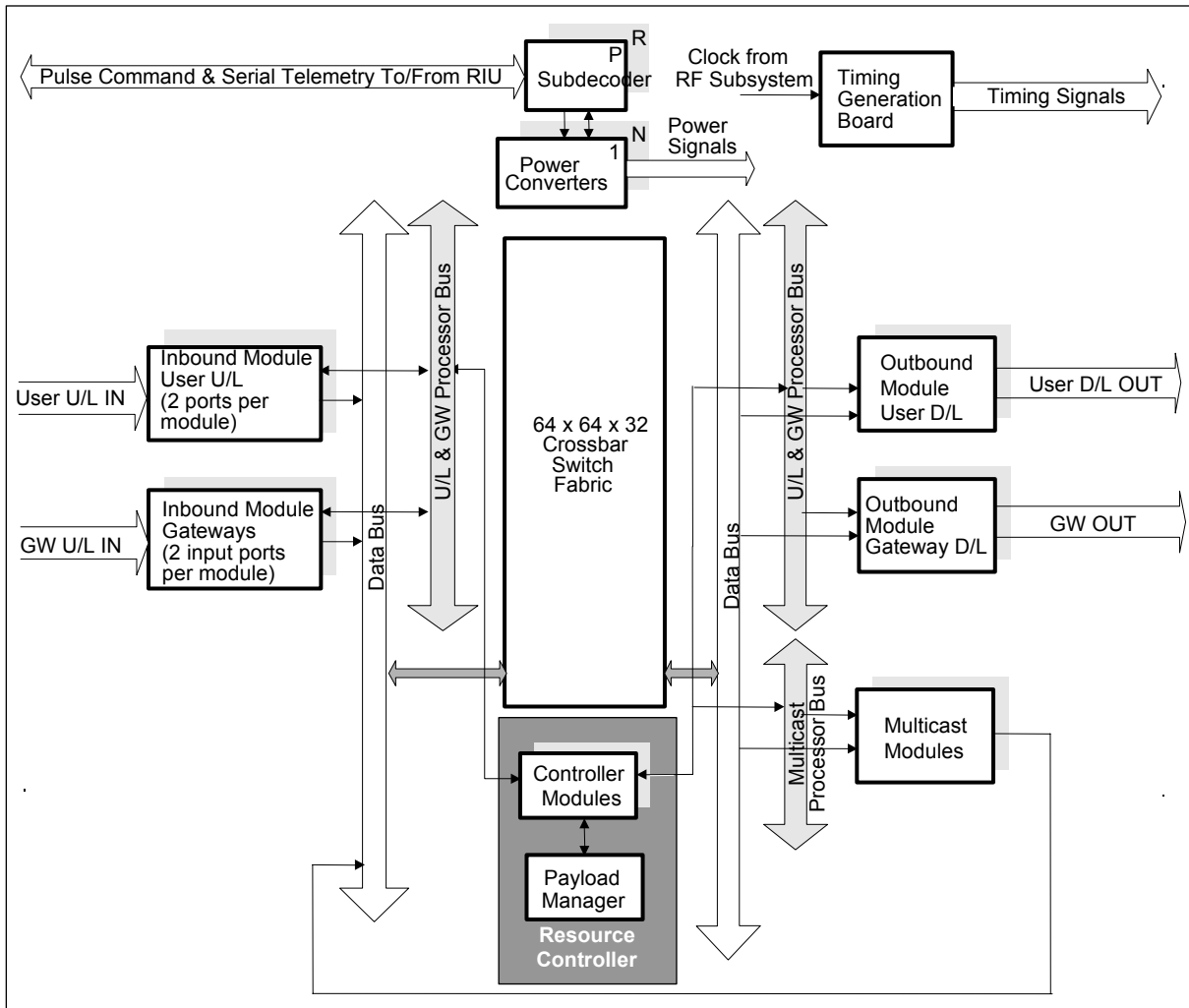
The following sections discuss the various architectural features of this broadband packet switch processor in greater detail.

**Figure 2. Satellite Network Concept of Operations**



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**Figure 3. Broadband Packet Switch Processor Architecture**



### INPUT ARCHITECTURE

The architecture of the broadband packet switch processor's input emphasizes the preprocessing of incoming ATM cell traffic of various connection types in preparation for switching to their desired output port. Features of the input architecture include:

- Processing of three types of connections (virtual channel (VC), virtual path (VP), and connectionless) using table lookup - *flexibility*
- Remapping of received ATM header virtual channel identifier (VCI) to an output VCI—*enables address reuse and simplifies network control*
- Header error control (HEC), error check, and regeneration—*ensures data integrity*
- Accepts traffic from two demodulator outputs per input module—*enables more processing capability with less hardware; thus saving power and weight*

- Idle cell discard—*allows more efficient data traffic processing and preserves downlink bandwidth for useful data*
- Interface to onboard processor to process commands from the ground, e.g., call setup and/or tear-down and fault management
- Collection of statistics to facilitate performance monitoring and fault management. Parameters include number of cells received, number of cells dropped due to HEC error; queue occupancy and queue overflow; single bit error and double bit error counts and memory locations; and activity monitors for fault management and isolation.
- Arbitration of head of line (HOL) cell
- Scalable and expandable

The input architecture is easily scaled since it uses the same design for all types of input processing, user terminal or gateway terminal. The architecture is easily adapted to

the specific needs of a network. The number of input processing modules can be increased or decreased as needed to support increasing or decreasing numbers of uplink beams without affecting other parts of the packet switch processor. Each input module's capability to interface to and process data from two demodulators simultaneously saves power and weight aboard the satellite.

### **ARBITRATION AND SWITCH FABRIC ARCHITECTURE**

ATM cells are routed across a 64 x 64 self-routing, non-blocking crossbar switch fabric that forms the heart of the packet switch processor. Any input port can route to any output port. The switch uses a speedup factor to minimize contention. Each input processing module can process two data outputs from two uplink beams simultaneously. Similarly, each output processing module is also capable of processing data for two downlink beams; thus, the architecture can have up to 128 input ports and 128 output ports.

A central arbitration scheme is an integral and necessary part of this architecture to resolve any conflicts that may arise when more than one input port wants to send data to the same output port simultaneously. The fair arbitration algorithm is optimized to minimize the probability of input queuing congestion while still ensuring no ports are starved for service.

### **OUTBOUND ARCHITECTURE**

The architecture of the broadband packet switch's output emphasizes the post-processing of ATM cell traffic for downlink transmission. The architecture is optimized for a space-based application using large cell buffers to feed the downlink beams to minimize dropped cells due to congestion. Features of the output architecture includes:

- Queuing by downlink priority and adaptive coding type
- Multi-level downlink priorities based on QoS needs—accommodates up to 512 different queues and supports fair-weighted queuing
- Multiple coding modes for weather conditions— heavy coding for rain or storm conditions and light coding for clear weather
- Flexible downlink frame forming—supports fair-weighted queuing algorithms, processes data for two downlink beams simultaneously, and reconfigures the downlink scheduling table based on ground and onboard processor commands
- HEC—error check ensures data integrity
- Network congestion control—prevents loss of high priority data due to traffic congestion—uses cell loss priority (CLP) bit for cell discard and supports

early packet discard (EPD)

- Multiple modes of queue structure—dynamic link list structure maximizes flexibility of queue space and priority data processing; fixed partitioning structure guarantees queue space for all priorities
- Statistics collection enables performance monitoring and fault management. Parameters observed include queue occupancy, queue thresholds,-peak cell count; CLP and EPD cell discard counts, amount of free cell space in queue, number of cells transmitted and activity monitors for fault management and isolation
- Scalable and expandable

The output architecture is easily scaled since it uses the same design for all types of output processing both to a user terminal or to a gateway terminal. The architecture is also easily adaptable to the needs of the network. The number of output processing modules can be increased or decreased as needed with changes in the number of downlink beams without affecting other parts of the packet switch processor. Each module's ability to process data for, and interface to, two downlink beams simultaneously leads to power and weight savings onboard the satellite.

### **MULTICAST ARCHITECTURE**

Maximum efficiency in the use of uplink bandwidth is achieved by including multicast capability aboard the satellite. Source terminals need only send the data once to the satellite and then let the onboard packet switch processor perform the duplication of the data cells, thereby allowing the uplink bandwidth to be used efficiently. The multicast architecture is a cross between input and output architectures. Its input comes from the switch fabric output port, and its output goes to the switch fabric input port. The multicast architecture features include:

- ATM cell replication for transmission to multiple destinations—allows efficient usage of uplink bandwidth
- HEC error check and generation—ensures data integrity
- Processing of three types of connections (VC, VP, and connectionless) using table lookup—offers flexibility
- Interface to onboard processor to processes commands from the ground, e.g., multicast traffic call setup and/or tear-down, addition or deletion of multicast destinations, and fault management
- Collection of statistics to facilitate performance monitoring and fault management. Parameters include number of cells received and/or cells dropped due to HEC error; number of cells duplicated; queue occupancy and queue overflow; single bit error and double bit error counts and memory locations; and activity monitors for fault management and isolation
- Arbitration of HOL cell
- Scalable and expandable

The multicast architecture, like the input and output architectures, is easily scalable and expandable. Its

implementation will not affect changes to other parts of the overall switch architecture.

### **DESIGN APPROACH**

Supporting 70+ beams and >10 GBPS throughput requires extremely dense packaging including the use of advanced microelectronics. Complex, multi-million gate, sub-micron complementary metal oxide semiconductor (CMOS) application specific integrated circuits (ASICs) make onboard processing realizable within the satellite's weight and power allocation. TRW has developed a design methodology over four generations of digital processors that ensures "first pass success" of the ASIC designs. This methodology includes extremely thorough and rigorous design verification prior to design hand-off to the foundry, early functional prototyping of multi-ASIC functions, and use of advanced tools to ensure all the intricacies of sub-micron CMOS design are accounted for.

Traditional functional testing will not ensure adequate fault coverage. For this reason, BIST is incorporated into the designs allowing thorough and rapid test at both piece-part and unit level. The complexities of ASIC designs are mitigated by the measures taken during design flow. The unit architecture supports line replaceable modules (LRMs). Each individual module is replaceable at the payload level without impacting other modules.

### **SUMMARY**

TRW's Gen\*Star broadband high-speed packet switch processor addresses the future needs of the broadband regenerative (processed) payload market. The architecture allows maximum flexibility as well as maximum scalability. A variety of applications and services can be accommodated by this architecture. Units have successfully completed flight qualification.