



# GaAs IC Die Handling, Assembly and Testing Techniques

Note: The data contained in this document is for information only. Northrop Grumman reserves the right to change without notice the specifications, designs, prices or conditions of sale, as they apply to this product. The product represented by this datasheet is subject to U.S. Export Law as contained in ITAR or the EAR regulations.

**1. Scope**

This document describes the storage and handling requirements for GaAs IC chips. It also describes recommended assembly and testing techniques for users of GaAs IC chips. Chips are usually delivered to the end user as individual chips stored in plastic chip trays or GelPax. This document provides guidelines to aid the user in the assembly of GaAs IC die in a manner consistent with desired electrical performance.

**Note:** The information given herein is based upon data believed to be reliable. Northrop Grumman Space Technology (NGST) makes no warranties expressed or implied as to its accuracy, and assumes no liability arising out of its use by others. This publication is not to be taken as a license to operate under, or recommendation to infringe, any patents.

**1.1 Organization of Document**

This document addresses the following areas:

- Packaging for shipment: Paragraph 3.1
- Allowable storage conditions: Paragraph 3.2
- Recommended assembly processes: Paragraph 3.3
- External Components: Paragraph 3.4
- Electrostatic discharge sensitivity (ESD): Paragraph 3.5
- Electrical overstress sensitivity (EOS): Paragraph 3.6

**2. Applicable Documents**

The “MIL\_STD\_883, Test Methods and Procedures for Microelectronics” is referenced in this document.

**3. Handling Requirements and Process Recommendations****3.1 Packaging for Shipment**

GaAs is a relatively brittle material without the exceptional strength associated with silicon crystals. Furthermore, the chips may be as thin as 2 mils (50 microns) at their thickest point. Due to this, it is necessary to treat GaAs chips with far more care than that is required for silicon ICs. Chips are packaged in Fluoroware (or equivalent) anti-static chip trays or GelPak boxes. The container is wrapped in a shock absorbent material, such as bubble-pack prior to boxing the shipment.



## 3.2 Allowable Storage Conditions

Compared to many other microelectronic devices, GaAs chips are relatively durable under a wide range of storage environments. NGST's GaAs ICs have no exposed materials that can easily corrode or degrade. All exposed metallizations are gold, and all active devices are passivated with silicon nitride. It is obviously essential that the storage environment be free of any substance that can degrade these materials. Long-term exposure to concentrated agents capable of corroding GaAs or other metals is also not recommended, since the passivation layers are thin and not completely impervious.

### 3.2.1 Recommended Atmosphere

Although not necessary, a clean, dry nitrogen atmosphere is recommended for storage. Normal ambient air will not damage GaAs devices, but if the chips are allowed to become wet or dirty, they will be difficult to clean.

### 3.2.2 Storage Temperatures

NGST's GaAs ICs are recommended to be stored at room temperature ( $25^{\circ} \pm 3C$ ). NGST's GaAs ICs can be stored at  $125^{\circ}C$  indefinitely without damage. GaAs chips are capable of surviving much higher temperatures for shorter times.

## 3.3 Recommended Assembly Process

Figure 1 shows a typical GaAs IC chip assembled.

### 3.3.1 Individual Chip Handling

The metallization patterns on the frontside of the chip are very fragile. Any tool that contacts the frontside of the the chip, must be used with extreme caution. Vacuum pickup tools may be used on GaAs chips, but NGST recommends that they be used only on the backside of the chip. It is recommended to use ESD composite tweezers.

**Note:** Many of the NGST parts do incorporate airbridges, so caution should be used when determining the pick up tool.

### 3.3.2 Personnel Training

Assembly operators familiar only with silicon ICs, ceramic substrates, or even GaAs FETs, should be retrained specifically for handling GaAs chips. NGST has learned that many people hired without previous GaAs experience require a period of training and practice before they can safely and confidently handle GaAs chips.

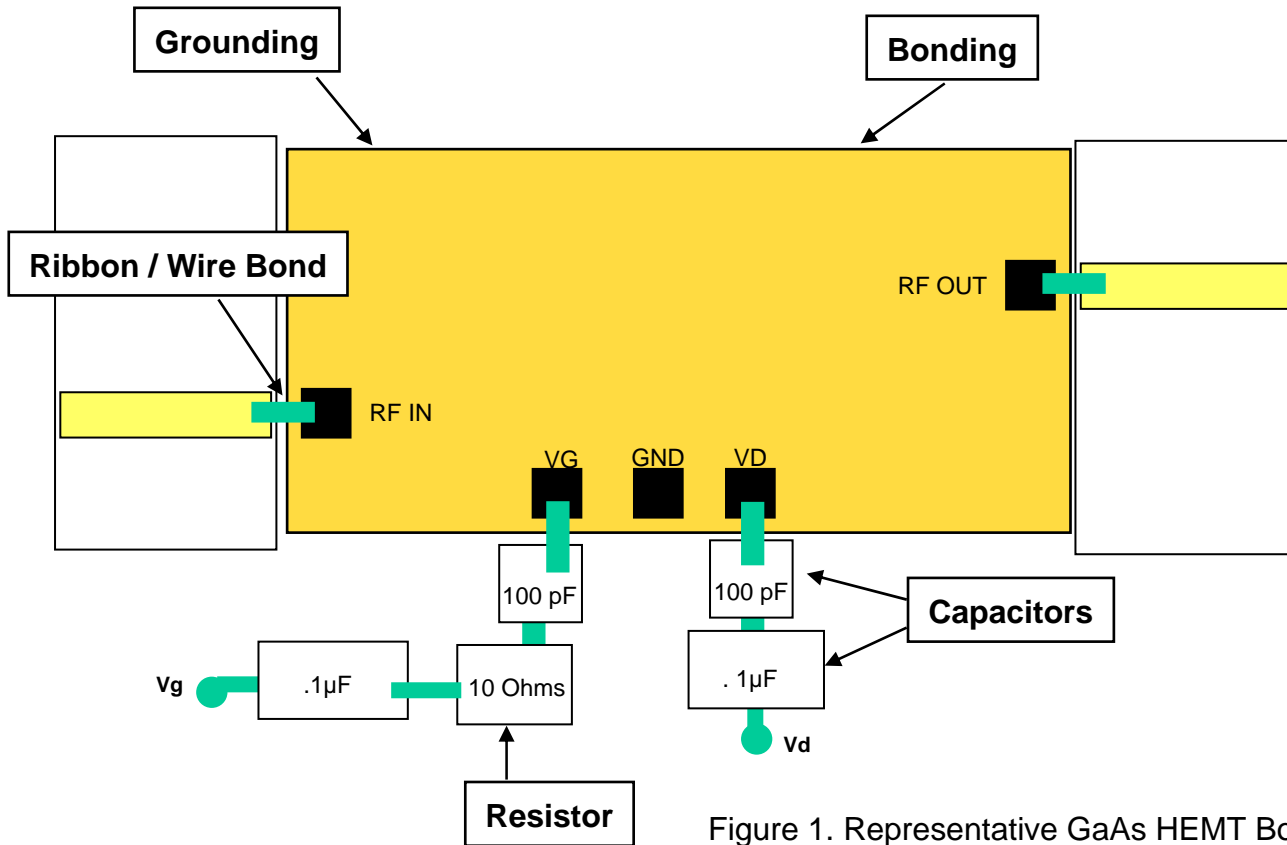


Figure 1. Representative GaAs HEMT Bonding

### 3.3.3 Mounting Processes

Most NGST GaAs IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGST recommends the use of conductive epoxy due to the reduced mechanical strain placed on the chip. The two most important factors when mounting these MMICs are to provide a good thermal path and a good RF path to ground. This should be considered when determining the method for attachment.

Possible Materials include:

- Eutectic Attachment
- Silver Epoxy

**Note:** Many of the NGST parts do incorporate airbridges, so caution should be used when determining the pick up tool.

**CAUTION:** THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaAs CHIPS. THE DECISION TO USE AuSn ATTACHMENT AND THE RESPONSIBILITY FOR ANY RESULTING DAMAGE RESTS SOLELY WITH THE END USER.

Note: The data contained in this document is for information only. Northrop Grumman reserves the right to change without notice the specifications, designs, prices or conditions of sale, as they apply to this product. The product represented by this datasheet is subject to U.S. Export Law as contained in ITAR or the EAR regulations.



### 3.3.4 Grounding

The back of the chip is the ground plane so it is imperative that it sees a good ground connection. Without good grounding the chip could see an increased inductance and/or resistance to ground. The result of this is the potential for oscillations.

It is recommended to mount the part straight to a thermally matched metal carrier (which will inherently provide a good path to ground). Another option is to mount it onto a substrate, which itself is mounted to the carrier plate. If the chip is to be mounted to a substrate the grounding becomes critical. You need to insure that there are multiple ground vias, so as the top of the substrate now appears as a solid ground plane. Filled vias should always be used to help prevent resonance between grounds and to provide a good thermal interface.

The Ground pads on the chip are for wafer probing only. They do not require being bonded. The On chip Ground pad SHOULD NOT be used as an alternative to providing the back plane with an adequate ground.

### 3.3.5 Ribbon/Wire Bonding

NGST GaAs IC chips have gold metallization on all bond/probe pads and are therefore suitable for both gold wire and ribbon bonding. When a proper bonding schedule is used, the bond strength and pad adhesion are capable of meeting the destructive bond pull limits in MIL\_STD\_883.

To attach the RFIN / RFOUT pads to the substrate either a ribbon or a wire can be used. The lengths should be kept to a minimum to limit the inductance and possible affect it can have on the performance of the chip. The preferred method is to use a wedge bond.

The first Ribbon/Wire in the bias line (from the chip to the 100pF cap) is the most critical. If a long wire is used, it could form a series resonance with the 100pF cap and cause an oscillation.



**3.3.5 Ribbon/Wire Bonding (cont.)**

**General recommendations for wire/ribbon bonding are:**

- a. Ball bonding is not recommended for signal path bonds. If a ball bonder is used on the DC lines, then a keep out zone of 0.5” for the flame-off feature is recommended.
- b. The safest, most reliable technique utilized at NGST, is a thermosonic wedge bonder. This is more user and ESD friendly.
- c. Provide proper grounding for the bonder equipment and all peripheral equipment, including heated stages and wire feeds.
- d. Use an oscilloscope to check for the voltage at the bonding tip of the wire bonding equipment. Check the voltage with the wire or ribbon in place.
- e. The tooling recommendations for gold wire and gold ribbon are listed in Table I.
- f. Metal pads tend not to adhere as well to GaAs as they do to other substrates (e.g.silicon). Therefore, it is even more critical in GaAs assembly to establish a proper bond schedule; too little power applied will result in a weak bond. On the other hand, too much power may damage the pad and even delaminate the pad from the substrate. Please check the guidelines for your specific machine.
- g. Ground substrate bonding pads, traces and capacitors before bonding to sensitive devices. Remove these wires before electrical testing.
- h. Back bond whenever possible. This means bonding to grounded substrate pads before bonding to device bond pads, and bonding to DC bond pads before RF bond pads. Back bonding effectively provides a ground path for any voltage on the bonding tip.

**Table I. Gold Wire/Ribbon Description and Tooling**

	<b>Gold Wire</b>	<b>Gold Ribbon</b>
<b>Use</b>	Low Frequency signal paths and DC	RF signal paths
<b>Size</b>	1 mil diameter	3mils wide x 0.5 mils thick
<b>Minimum Elongation *</b>	3.0%	3.0%
<b>Minimum Breaking Load**</b>	3.5 grams	5 grams

\*Minimum Elongation is application specific.

\*\* Minimum Breaking Load is per MIL Standard

Note: The data contained in this document is for information only. Northrop Grumman reserves the right to change without notice the specifications, designs, prices or conditions of sale, as they apply to this product. The product represented by this datasheet is subject to U.S. Export Law as contained in ITAR or the EAR regulations.



### 3.4 External Components

These are the recommended off chip bias components to insure that the electrical performance of the chip matches the performance as seen in the data sheets.

#### 3.4.1 Capacitors

**1. 100pF Cap**

The first bias bypass capacitor should be a 100pF (approx.) ceramic (single layer) capacitor, placed no farther than 30 mils from the MMIC.

**2. 0.1uF**

The second bias bypass capacitor helps to eliminate any other very low frequency problems.

\*Note: If you are tying multiple gates/drains together, the best place to tie them together is at the 0.1uF capacitor. This will help to prevent instability.

#### 3.4.2 Resistors

**1. 10 Ohm Resistor**

The resistor on the gate line is used to DQ the bias line.

### 3.5 Electrostatic Discharge Sensitivity

Electrostatic discharge(ESD) refers to excessive voltage applied to a chip, generally as a result of contact with an ungrounded human body. ESD damage thresholds measured on a variety of NGST GaAs devices per MIL-STD-883, Method 3015 (Human Body Model) are listed in Table II. GaAs chips tend to have a lower ESD threshold than do silicon devices, and unlike silicon, most of these devices have no built in ESD protection. The data in Table II is thought to represent the worst-case, or most sensitive circuit topology. At NGST all GaAs IC products are treated and handled as ESD sensitive Class 1, both during and after the time the individual chips are diced out of the wafer. The risk of ESD damage to the chips while they are still in wafer form is actually small, except during probe testing. During probe testing, electrostatic discharges could be applied to the sensitive device terminals through the probes.



Recommended procedures for preventing ESD damage are listed below:

- Adequately train personnel in the prevention of ESD damage before they handle GaAs devices.
- Follow ESD prevention procedures throughout assembly and test. Use pin-to-case grounding, or pin shielding, or back bonding (see paragraph 3.3.4) whenever possible.
- Store GaAs chips and wafers in anti-static containers. For chip trays, also known as waffle packs), NGST recommends Fluoroware STAT-PRO 400 trays.
- Ensure that all equipment is properly grounded and isolated from each other.
- Handle GaAs chips only at workstations properly equipped with ESD-prevention products and materials (e.g. grounded wrist straps, grounded table tops, etc.)

**Table II. Damage threshold from Electrostatic Discharge  
(MIL-STD-883, Method 3015)**

<b>Device</b>	<b>Damage Threshold Positive Polarity (V)</b>	<b>Damage Threshold Negative Polarity (V)</b>
GaAs 0.5um MESFET (MMIC)	>650	<500
GaAs 0.2um Low-Noise HEMT (discrete)	>175	50-70
GaAs 0.15um Power-HEMT	*	*
GaAs 0.1um Low-Noise HEMT	*	*
GaAs 3um Emitter-HBT (discrete)	*	*
GaAs 2um Emitter-HBT (discrete)	250-525	50-125
GaAs 1um Emitter-HBT	*	*
* No data at this time		

### 3.6 Electrical Overstress Sensitivity

Electrical overstress sensitivity (EOS) damage results from an excessive voltage applied to the terminals of a chip. GaAs chips tend to have a lower EOS damage threshold than do silicon devices. Typical EOS damage threshold measurements on discrete GaAs devices are shown in Table III. EOS damage often occurs during testing, test set operators must be adequately trained in proper test methods in order to prevent damage to GaAs devices. EOS can also occur during wirebonding if a high voltage exists at the wire bond tip, or bonding tool stage. Listed below are some guidelines for GaAs device testing and wire bonding:

- Always check chip orientation before eutectic or epoxy attach.
- Know your devices' breakdown voltages

Note: The data contained in this document is for information only. Northrop Grumman reserves the right to change without notice the specifications, designs, prices or conditions of sale, as they apply to this product. The product represented by this datasheet is subject to U.S. Export Law as contained in ITAR or the EAR regulations.



- c. Use a power supply with both voltage and current limit.
- d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
  - Apply bias (e.g. Negative gate voltage for FET/HEMT devices) to ensure that the device is off if applicable.
  - Apply supply voltages to set the chosen operating point.
- e. Use an oscilloscope to check the voltage at the bonding tip of wire bonding equipment. Use a multimeter to check the resistance from the bonding tip and stage of the wire bonder to ground. Ensure that all bonding equipment which comes into contact with the device/IC is grounded. Perform regular periodic checks of all equipment as part of a preventative-maintenance program.

**Table III. Damage Threshold from Electrical Overstress (DC)**

Device	Max Forward Voltage (V)	Current at Max Forward Voltage (mA)	Max Reverse Voltage (V)	Current at Max Reverse Voltage (mA)
GaAs 0.5um MESFET (300um)	3.9	244	19.3	31.3
GaAs 0.2um Low-Noise HEMT (200um)	3.4	160	9	0.67
GaAs 0.15um Power-HEMT (200um)	2.9	74	9.7	0.12
GaAs 0.1um Low-Noise HEMT	*	*	*	*
GaAs 3x10um Emitter-HBT	2.5 Vbe 2.5Vbc	70Ibe 80Ibc	9Vbe 25Vbc	9Ibe 1Ibc
GaAs 2x10um Emitter-HBT	2.5 Vbe 2.5Vbc	60Ibe 80Ibc	*	*
GaAs 1um Emitter-HBT	*	*	*	*
* No data at this time				

Note: The data contained in this document is for information only. Northrop Grumman reserves the right to change without notice the specifications, designs, prices or conditions of sale, as they apply to this product. The product represented by this datasheet is subject to U.S. Export Law as contained in ITAR or the EAR regulations.



**Table IV. Summary of NGST's GaAs IC Handling Recommendations**

	<b>Recommended Practice</b>	<b>Comments</b>
<b>Packaging Chips</b>	Store in individual chip trays (Fluoroware, STAT-PRO 400, or equivalent).	
<b>Storage General</b>	Avoid exposure to corrosive materials.	Exposed surfaces (gold and silicon nitride) are corrosion resistant, but still require careful handling.
<b>Atmosphere</b>	Store in dry nitrogen.	Normal air is not damaging, but care must be taken to avoid chips becoming wet or dirty.
<b>Temperature</b>	Store below 125C.	Chips can withstand higher temperatures for short periods of time.
<b>Assembly Chip Handling</b>	Use extreme caution with tools that contact the frontside of the chip.	Verify that any vacuum pick-up tool which contact the front of the chip do not cause damage, or only use tools against the backside of the chip.
<b>Training</b>	Personnel require training and practice to safely handle GaAs chips.	Previous experiences with silicon IC chips or ceramic substrates does not qualify for GaAs chips.
<b>Mounting</b>	Mount with conductive epoxy.	AuSn attachment is not recommended, but can be used with the restriction listed in Paragraph 3.3.3.
<b>Wire Bonding</b>	Manual, wedge-wedge gold ribbon bond tool, with no flame-off feature. Employ back bonding where possible.	Ball bonding is not recommended.
<b>Electrostatic Discharge Protection</b>	Follow recommendation in Paragraph 3.5	Treat all GaAs IC chips as Class 1 ESD sensitive.
<b>Electrical Overstress Protection</b>	Follow recommendation in Paragraph 3.6. Always check the voltage on the bonding tip with an oscilloscope before bonding. Ensure that the test set power supply will not exceed the devices's limits.	Wire bonding equipment can generate dangerous voltages at the tip or stage. Monitor all bonding equipment regularly.

Note: The data contained in this document is for information only. Northrop Grumman reserves the right to change without notice the specifications, designs, prices or conditions of sale, as they apply to this product. The product represented by this datasheet is subject to U.S. Export Law as contained in ITAR or the EAR regulations.